Amendments to the Claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): Testing system for use in testing a system-under-test (SUT), the testing system comprising:

a first logic section that may transmit one or more test-related signals for use during a test mode of the SUT;

a second logic section that may transmit one or more other signals during a normal operating mode of the SUT; and

a third logic section that selectively couples one of the first logic section [[and]] or the second logic section to the SUT based upon respective assertion states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

wherein:

when the third logic section couples the first logic section to the SUT, the first logic section [[may]] transmits the one or more test-related signals to the SUT, and when the third logic section couples the second logic section to the SUT, the second logic section may transmit the one or more other signals to the SUT.

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Claim 2. (previously presented) The testing system of claim 1, wherein the first logic section comprises built-in-self-test (BIST) logic and the one or more test-related signals comprise test input signals for use in testing the SUT.

Claim 3. (currently amended) The testing system of claim 1, wherein the first logic section [[may]] provides an indication signal to the second logic section for indicating when the first logic section is attempting to test the SUT.

Claim 4. (previously presented) The testing system of claim 3, wherein the second logic section [[may]] provides to an input/output (I/O) controller an indication that the testing of the SUT is occurring, the I/O controller being external to the first logic section, the second logic section, the third logic section, and the SUT.

Claim 5. (currently amended) The testing system of claim 4, wherein, in response to the indication from the second logic section, the I/O controller [[may]] causes a data transfer occurring contemporaneously with the testing of the SUT to be invalidated.

Claim 6. (currently amended) The testing system of claim 1, wherein the respective assertion state of the one of the two control signals [[may be]] is selected.

Claim 7. (previously presented) The testing system of claim 1, wherein:

when the third logic section couples the first logic section to the SUT, the first logic section may receive one or more test outputs from the SUT, the one or more test

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output signals being generated by the SUT in response to the one or more test-related signals, and the first logic section may compare the one or more test outputs to one or more expected test outputs whereby to determine results of the testing.

Claim 8. (previously presented) The testing system of claim 1, wherein:

if both of the control signals are asserted, the third logic section couples the first logic section to the SUT;

if at least one of the control signals is unasserted, the third logic section couples the second logic section to the SUT.

Claim 9. (previously presented) The testing system of claim 1, wherein:

the SUT comprises a memory; and

the second logic section may be used in causing the memory to store an erroneous value that may be detected during the testing.

Claim 10. (currently amended) Testing system for use in testing a plurality of systems-under-test, the testing system comprising:

a first logic section;

a plurality of second logic sections;

a plurality of third logic sections;

each respective third logic section being coupled to the first logic section and to a respective second logic section, and being configured to selectively couple ~~one of~~ the first logic section [[and]] or the respective second logic section to a respective system-under-

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test based upon a respective control signal from the first logic section and also based

upon another control signal, the another control signal being transmitted to each third

logic section from a source that is external to the plurality of systems-under-test, the first

logic section, the plurality of second logic sections, and the plurality of third logic

sections;

wherein:

when the first logic section is coupled to the respective SUT, the first logic

section [[may]] transmits one or more test-related signals to the respective

SUT, and when the respective second logic section is coupled to the

respective SUT, the respective second logic section may transmit one or

more respective other signals to the respective SUT.

Claim 11. (previously presented) The testing system of claim 10, wherein the testing

system is comprised in an application specific integrated circuit (ASIC), and the source is

external to the ASIC.

Claim 12. (previously presented) The testing system of claim 11, wherein:

the first logic section comprises programmable built-in-self-test logic, and the

first logic section is coupled to each of the third logic sections and to each of the second

logic sections.

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Claim 13. (currently amended) Method of using a testing system for testing a system-under-test (SUT), the testing system including a first logic section, a second logic section, and a third logic section, the method comprising:

selectively coupling, via the third logic section, ~~one of~~ the first logic section [[and]] or the second logic section to the SUT based upon respective assertion states of two control signals, one of the two control signals being transmitted to the third logic section from a source that is external to the SUT, the first logic section, the second logic section, and the third logic section, the other of the two control signals being transmitted to the third logic section from the first logic section;

transmitting to the SUT from the first logic section, when the first logic section is coupled to the SUT via the third logic section, one or more test-related signals; and

transmitting to the SUT from the second logic section, when the second logic section is coupled to the SUT via the third logic section, one or more other signals to the SUT.

Claim 14. (previously presented) The method of claim 13, wherein the first logic section comprises built-in-self-test (BIST) logic and the one or more test-related signals comprise test input signals for use in testing the SUT.

Claim 15. (previously presented) The method of claim 13, further comprising, providing from the first logic section an indication signal to the second logic section for indicating when the first logic section is attempting to test the SUT.

Claim 16. (previously presented) The method of claim 15, further comprising, providing

from the second logic section an indication to an input/output (I/O) controller that the

testing of the SUT is occurring, the I/O controller being external to the first logic section,

the second logic section, the third logic section, and the SUT.

Claim 17. (previously presented) The method of claim 16, wherein, in response to the

indication from the second logic section, the I/O controller causes a data transfer·

occurring contemporaneously with the testing of the SUT to be invalidated.

Claim 18. (previously presented) The method of claim 13, wherein the respective

assertion state of the one of the two control signals may be selected.

Claim 19. (previously presented) The method of claim 13, further comprising:

receiving at the first logic section, when the third logic section couples the first

logic section to the SUT, one or more test outputs from the SUT, the one or more test

outputs being generated by the SUT in response to the one or more test-related signals;

and

comparing at the first logic section the one or more test outputs to one or more

expected test output signals.

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Claim 20. (previously presented) The method of claim 13, wherein:

 if both of the control signals are asserted, the first logic section is coupled via the

third logic section to the SUT; and

 if at least one of the control signals is unasserted, the second logic section is

coupled via the third logic section to the SUT.

Claim 21. (previously presented) The method of claim 13, wherein:

 the SUT comprises a memory; and

 the method further comprises using the second logic section to cause the memory

to store an erroneous value that may be detected by the first logic section during the

testing.

Claim 22. (currently amended) Method of using a testing system that may be used to test

a plurality of systems-under-test, the testing system including a first logic section, a

plurality of second logic sections, and a plurality of third logic sections, each respective

third logic section being coupled to the first logic section and to a respective second logic

section, the method comprising:

 configuring each respective third logic section to selectively couple one-of the

first logic section [[and]] or the respective second logic section to a respective system-

under-test based upon a respective control signal from the first logic section and also

based upon another control signal, the another control signal being transmitted to each

third logic section from a source that is external to the plurality of systems-under-test, the

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first logic section, the plurality of second logic sections, and the plurality of third logic

sections;

transmitting from the first logic section, when the first logic section is coupled to

the respective SUT, one or more test-related signals to the respective SUT; and

transmitting from the respective second logic section, when the respective second

logic section is coupled to the respective SUT, one or more respective other signals to the

respective SUT.

Claim 23. (previously presented) The method of claim 22, wherein the testing system is

comprised in an application specific integrated circuit (ASIC), and the source is external

to the ASIC.

Claim 24. (previously presented) The method of claim 23, wherein:

the first logic section comprises programmable built-in-self-test logic, and the

first logic section is coupled to each of the third logic sections and to each of the second

logic sections.

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